DMS LAB Limited

20V BiCDMOS process specification

› Description

- 20V 2.0um BiCDMOS process is DMS Lab Limited BCD smart power technology.
- Main target applications are analog switch ICs, DC-DC converters, driver ICs for capacitive, inductive and resistive loads for applications using 20V supply. The typical breakdown voltage of the lateral DMOS devices more than 20V.
- The modular process combines DMOS and HV CMOS for different supply application with core bipolar, logic CMOS processing steps to provide a wide variety of MOS and bipolar devices with different voltage levels on the same die.
- The 18 layers core process module is available for 20V breakdown voltage of the DMOS. This process module provides locos insulation, one level poly, and two metal levels.

  With this core module an optimized n-channel lateral DMOS transistor, HV CMOS, logic CMOS and some bipolar transistors can be made,

1	**Wafer**	
1	**N+buried**	
2	**P+buried**	
	Epi	
3	**Well 1**	
4	**Well 2**	
5	**Well 3**	
6	**Active**	
7	**P-guard**	
8	**Deep Drain**	
9	**Ch.adjust**	
10	**Gate**	
11	**P-body**	**HV Poly**
12	**P+Drain**	
13	**N+Drain**	
14	**Contact**	
15	**Metal 1**	
16	**Via**	
17	**Metal 2**	
18	**Pad**	

- One more process modules can be added to integrate high value poly-Si resistors and PIP capacitors (1 layer).

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> Key Features

The lateral DMOS transistor with low Rdson and small area is the main HV component of the BiCDMOS 20V technology.

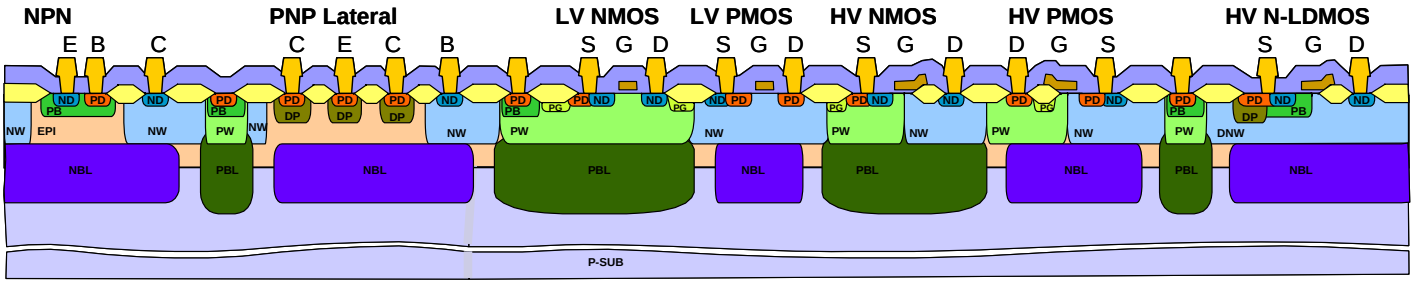
2.0um one poly, double metal, triple Well BCD process.

A high number of different devices are available:

- 20V n-channel lateral DMOS transistor;
- 20V n-channel MOS transistor;
- 20V p-channel MOS transistor;
- Logical 5V CMOS transistors;
- 20V NPN transistors;
- 20V PNP transistors;
- Zener diodes and Schottky diodes;
- Gate oxide capacitors;
- Low resistivity poly-Si resistors;
- Resistors in active layers.
    - Optional poly for high value resistor;
    - Optional poly-1 – poly2 capacitors;

> Schematic cross section

20V BiCDMOS



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> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area (CMOS)	2.0	0.8
CMOS Gate	2.0	2.0
DMOS Gate	2.0	--
Contact	2.0	1.0
Metal-1	2.5	1.5
VIA	2.0	2.0
Metal-2	2.5	2.0

〉 Device Parameters of main elements for 20V process

ELEMENT	PARAMETER	SPEC		MEASUREMENT CONDITIONS
	UNIT	MIN	MAX	
HV NDMOS L=2.0 um, W=40 um	VTH, V	0.7	1.3	Id=0.1uA
	IDS, mA	8.0	-	Ug=Ud=5 V
	BVDS, V	20	-	Id=10uA
	Rsp, mOhm*mm2	-	50	Ug=50 V
	IDS, uA	-	50	Ug=Ub=Us=0 V, Ud =20 V
HV NMOS L=4 um, W=50 um	VTH, V	0.5	0.9	Id=0.1uA
	IDS, mA	3	-	Ug=Ud=5 V
	BVDS, V	20	-	Id=10uA
HV PMOS L=5 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	1.0	-	Ug=Ud=5 V
	BVDS, V	20	-	Id=10uA
LV NMOS L=2 um, W=50 um	VTH, V	0.5	0.9	Id=0.1uA
	IDS, mA	6	12	Ug=Ud=5 V
	BVDS, V	8.0	-	Id=10uA
LV PMOS L=2 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	4.0	7	Ug=Ud=5 V
	BVDS, V	8		Id=10uA
LV NPN Se=10x10 um2	BETA	30	100	Ib=10uA, Uc=1 V
	BVCE0, V	20	-	Ic=10uA, floating base
LV Lateral PNP Wb=4um	BETA	20	-	Ib=-10uA, Uc=-1 V
	BVCE0, V	20	-	Ic=-10uA, floating base
Schottky Diode	BV, V	20	-	Id=10uA
Zener Diode	BV, V	5.5	6.5	Id=10uA
Base Resistor	RS, Ohm/sq	450	550	Ir=10uA
PolySi- gate oxide – Well capacitor	Ccs, pF/um2	1,2E-3	1.6E-3	F=1MHz, Vmea=5V
Note: ( ) – value for option (adding module)				